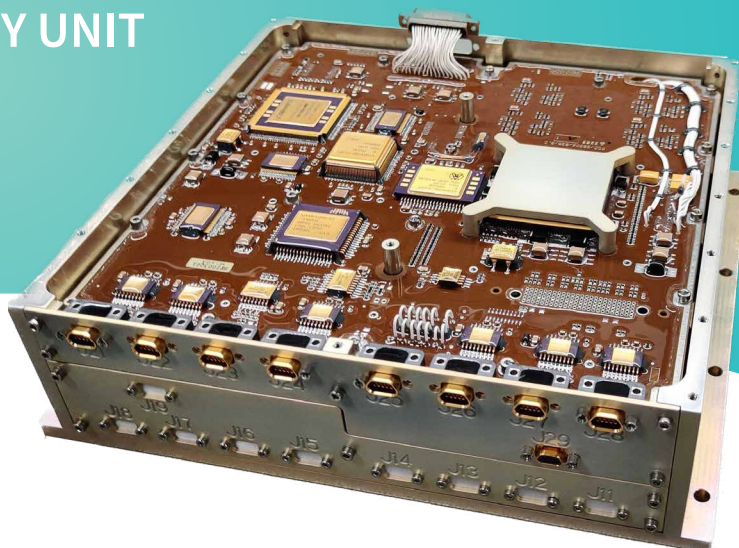


PERFORMANT MASS MEMORY UNIT



OVERVIEW

- Fully Qualified Architecture
- Leon 3 processor
- RTG4 FPGA including SpW Routing functionalities
- 5 / 8 (option) SpW interfaces at 100Mbps
- 2 LVDS downlink interfaces with Reed- Solomon processed CADU stream
- 512GBits / 1024GBits (option) of NAND FLASH of parallelized memories
- Embedded management of the memory (radiation protection, bad blocks, ...)
- Full SW PUS interface over SpW for the TM/TC
- 28V unregulated power supply
- < 15W power consumption
- TRL-7 (currently at EQM stage)

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