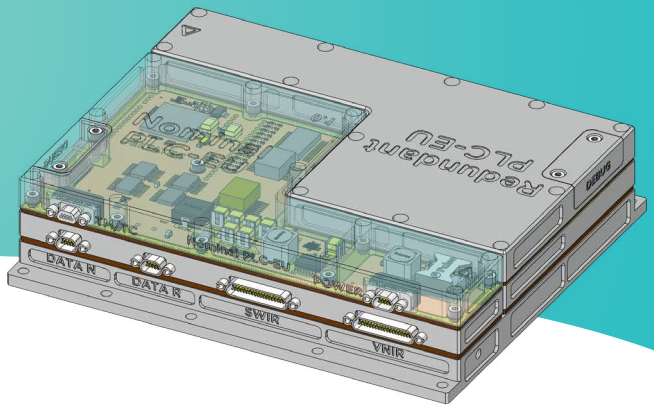
PRODUCT SHEET

NS PAYLOAD COMPUTER



OVERVIEW

- Dual payloads acquisition and local recording system
- Hybrid architecture (Cots + hardened components)
- Integrates radiation effects design mitigation technics
- ZynQ 7045 SoC with Dual Core ARM Cortex-A9 and Kintex-7 FPGA, 1024 GBytes of data storage
- Up to 6 LVDS I/F lines per payload at 100MHz

TECHNICAL CHARACTERISTICS

HARDWARE

- Single box offering cold electronic board redundancy, 2 identical electronic units are embedded into the box.
- Each unit is made of a data processing part and its dedicated radiation-hardened supervision part.
- Each unit offering:
  - o Processing part using defense-grade Xilinx Zync-7045 family (SoC with Dual Core ARM Cortex-A9 and Kintex-7 FPGA)
  - o Supervision part using radiation hardened processor.
  - o 1 Gbits of DDR3 memory with integrated ECC for fast data processing
  - o 2 Gbits of DDR3 memory with integrated ECC for slow data processing
  - o 256Mb Flash with Rad-Tolerant technology from 3DPlus for non-volatile storage of run-time journal.
  - o 512Mb Flash with Rad-Tolerant technology from 3DPlus for storage of processing unit firmware.
  - o 1TBytes (or more) On-board mass memory unit offering Rad-Tolerant Technology memory cells (SLC technology) for data storage.
- Compact and Modular design
  - o Same form factor for each redundant unit
  - o Data processing part and supervision part isolated as separate electronic boards.

RADIATION EFFECTS MITIGATION

- Design based on a hybrid approach (COTS components + Military Components + Rad Tolerant components + Radiation Hardened supervisor circuitry).
- On-board monitoring, detection, and mitigation of SEL (Single Event Latch-up).
- Continuous monitoring of processing parts by the Rad-Hard supervisor.
- Implementation of ECC for all memory peripherals (Flashes, DDR3 SDRAM and Mass Memory).
- SoC implements CRAM (Configuration memory) scrubbing mechanisms.
- Processing firmware upgradable in-flight over TM/TC link.

INTERNAL PROCESSING

- Acquisition start is time-programmable for precise control of first frames timestamp.
- Acquisition operations are able to grab frames simultaneously from both payloads interfaces or from a single sensor interface.
- Acquired data are recorded uncompressed and time-stamped in real-time to the internal mass memory.
- The on-demand download process is able to select a range of recorded data from mass-memory and push them to one of the 2 SpaceWire interface.
- Possible Hyperspectral on-the-fly compression for download using CCSDS-123.0-B-1 lossless algorithm which can offer up to 2x compression ratio.
- Each frame carries ANC data (can be customized).

HOUSE KEEPING

- Measurement of On-board Voltages by Rad-Hard supervision part (each power rail)
- Measurement of On-board Current consumption by Rad-Hard supervision part (each power rail)
- Measurement of On-board temperature (each PCB, and key components)
- Memory scrubbing status
- …

SIZE AND MASS

- Dimensions: 150x150x80mm
- Mass: < 2kg
- Housing material: Al6061-T6
- Surface finish: Surtec 650

INTERFACE

- Each of the 2 interfaces to payloads offers:
  - o 6 LVDS lines + 1CLK + 1 DataValid ingesting data interface, allowing up to 400 Mbits/s data throughput per payload.
  - o RS422 interface for TM/TC and housekeeping.
- Rugged Micro-D connectors for all interfaces.
- RS422 interface for TM/TC link with platform computer (control and housekeeping).
- A dual SpaceWire (200 MHz) interface for data download to ground (selectable) using CCSDS-133 space packet formatting.
- PPS input for on-board time synchronization and time stamping.

POWER SUPPLY

- 12VDC single power supply.
- From 15 to 35W power consumption, depending on internal processing

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